

AMENDMENTS TO THE ABSTRACT

A single loop PLL frequency synthesizer, ~~suitable for frequency applications~~ operation in the MHz ~~and to~~ GHz range, ~~suitable for integration in integrated circuits,~~ operates at high comparison frequencies ~~(on the order of 100 MHz and higher), with~~ excellent thus achieving superior phase noise performance, having wide loop bandwidths while able to tune in ~~but allows for small frequency steps. (on the order of 10 kHz or less), and is within Application Specific Integrated circuits (ASICs). The basic principle of operation of the Rational Frequency Synthesizer is that~~ It is based on the fact that the output frequency and the reference clock frequency always have a rational relationship, and so can (i.e. the ratio of the two frequencies can always be represented as a ratio of two integer numbers~~[[]]~~). This ratio ~~can always~~ is expanded into various expressions of equivalent fraction expansions. ~~The equivalent fractions take~~ taking the form of a series of divided, added or subtracted terms, each ~~term itself~~ being a rational number in itself. For each synthesized frequency, the computation of expansion terms yields specific, different values of the terms, with possibly multiple solutions. The ~~realization~~ This ratio is realized in hardware through stages of the computed fraction expansion terms is achieved by the means of a specific combination of frequency division and frequency translation (or frequency conversion) of the reference clock frequency and/or of the oscillator frequency. The above is accomplished through multiple consecutive up or down conversions of these frequencies, conversions using single sideband (SSB) mixers, ~~where (either the upper sideband (USB), or~~ [[the]] lower sideband (LSB), and ~~can be selected by the frequency control means in combination with~~

~~programmable frequency dividers, or counters. The converted and/or divided frequencies are compared in a phase detector, followed by a loop filter in a closed loop manner that provides phase locking of the oscillator. The realization in hardware of the above functions is accomplished by using bi-level (digital) circuits in combination with analog circuits. All necessary frequency control algorithms, instructions, design parameters and values are stored in non-volatile memory, and are used by an on-board controller or micro-processor to generate frequency control signals for the synthesizer's hardware. This process of frequency translation thus generates the comparison frequency to which the PLL phase-locks the VCO.~~